REMARKS/ARGUMENTS

Claims 1-2, 4-9, 12, and 14-18, and 20 remain pending in this application and stand rejected. Claims 3, 10-11, 13, and 19 are canceled rendering their rejections moot. Claims1-2, and 5-8, 12, 14, 16-18, and 20 are amended to clarify their respective languages.

In view of the foregoing amendments and following remarks, reconsideration of the rejections of claims 1-2, 4-9, 12, 14-18, and 20 is respectfully requested.

REJECTIONS UNDER 35 U.S.C. § 102

Claims 1-2, 4-7, 9, 12, 14, 16-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Anesko et al. (US 5,987,178). Applicants respectfully traverse these rejections for at least the following reasons.

Anesko et al. (hereinafter Anesko) is directed to motion estimation of video sequences. Anesko defines reference block and search area as described below:

> To estimate motion, the integral values of each block of pixels in a present frame (hereinafter called "reference block") is compared against the integral values of similarly-sized blocks of pixels in a region of a target frame (hereinafter called "search area") (1:67, 2:1-4)

It is noted that in the present application, a reference block is defined as the block that contains the search area (Anesko refers to this as "search area"). Support for this definition of reference block is provided, for example, on page 2, lines 17-21, page 6, lines 12-24; page 7, lines 26-34, page 8, lines 1-8. In other words, what Anesko defines as the search area is referred to in the present application as the reference block. Also, in the present application, a block to be motion compensated is referred to as the current block, as provided for example, on page 2, lines 17-21. In other words, what Anesko defines as the reference block is referred to in the present application as the current block.

To achieve motion compensation, Anesko reads rows (of pixels) of a block of the frame to be motion compensated, (referred to as current block in the present application and reference block in Anesko):

> In addition, the memory and PE array provide a pipelining mechanism that provides the ability to rotate the reference block within the array while it is running, and simultaneously read the memory contents into the array using a dual addressing mechanism (3:43-48)

There is no disclosure, however, in Anesko of performing motion compensation by reading rows and columns (of pixels) of the search area (referred to in the present application as the reference block). In other words, there is no disclosure in Anesko of "retrieving a block of pixels associated with a reference block from a reference frame memory; wherein said block of pixels includes NxM pixels wherein N represents the number of pixels in each row of the reference block and wherein M represents the number of pixels in each column of the reference block; and; storing said NxM pixels in a staging memory wherein said NxM pixels are rearranged and stored in the staging memory so as to form P groups each having L pixels such that during each read access cycle all L pixels of a different one of the P groups is read from the staging memory to a temporary memory; wherein each group of L pixels corresponds to a new row or a new column of said block of pixels" as recited, in part, in claim 1. Claim 1 and its dependent claims 2, and 4-9 are thus allowable over Anesko for this reason. Claims 12, and 14-18 are allowable for at least the same reasons as is claim 1.

Moreover, to perform motion compensation, Anesko only reads the rows of pixels, and fails to disclose reading the columns of pixels, as required in claim 1. As shown in Figs. 10 and 13 of Anesko, PE arrays 52 only read the pixels that are located along the rows of the search area. Referring to Fig. 5, index i in 1st stripe designated as s(0,1)-s(7,i), 2nd stripe designated as s(1,i)-s(8,i), and 3rd stripe designated as s(2,i)-s(9,i), refers to the row index of the pixels that are being processed. This processing appears to continue until the last row of the search area is reached, at which point, a read to the right and the top is shown as being made,

subsequent to which, the processing of the rows from top to bottom is repeated. This is also shown in Fig. 2 of Anesko:

> Thus, in this approach to calculating block differences, the pel stream alignment is shifted and the data is aligned in a pattern as shown in FIG. 5. As shown, for the first stripe, D(0,0), D(0,1), . . . D(0,21), the reference block is matched against the pel stripe 93 delineated with solid lines within the search region 85 shown in FIG. 2. For the second stripe D(1,0)(1,1), . . . , D(1,21), reference block is moved one pel to the right to match against the second pel stripe 94 delineated with dash lines in FIG. 2. This one pel shift per stripe is repeated until the last search stripe is shifted in. (3:66-67; 4:1-8)
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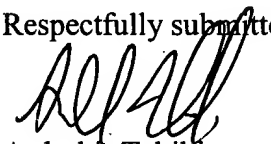
> Referring now to FIG. 10, there is shown a detailed view of the architecture of memory 55 and PE array 52. As shown, PE array 52 is a hardwired block-difference engine that consists of 8 rows of 8 absolute-difference-summing processing elements (ADS-Pe) 71, where each row is electrically connected to a final summation processing element (ADD-PE) 70.

Therefore, Anesko fails to disclose reading of pixels, along the columns, as recited, in part, in claim 1 "wherein each group of L pixels corresponds to a new row or a new column of said block of pixels". Claim 1 and its dependent claims 2, and 4-9 are thus allowable over Anesko for this reason. Claims 12, and 14-18 are allowable for at least the same reasons as is claim 1.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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